What is claimed is:

1. A line driver, comprising:

a signal input;

a peak detector receiving a digital data signal from the signal input and outputting a logic signal having a first logic value when the digital data signal exceeds a threshold value and a second logic value when the digital data signal is below the threshold value, said threshold value modifiable by an overhead value;

a data signal delay coupled to the digital data signal input and outputting a time-delayed digital data signal;

a DAC coupled to the signal input and receiving as input the time-delayed digital data signal and outputting an analog data signal;

a filter receiving as input the analog data signal and outputting a filtered analog data signal; and

an amplifier receiving as input the filtered analog data signal from the filter and the logic signal, the amplifier operating at a first operating voltage level when the logic signal is at the first logic value and operating at a second operating voltage level when the logic signal is at the second logic value.

2. The line driver of claim 1, wherein the peak detector outputs a third logic value when the digital data signal exceeds a second threshold value and further wherein the amplifier operates at a third operating voltage level when the peak detector outputs said third logic value.

3. The line driver of claim 1 further comprising a logic delay receiving as input said logic signal and outputting a time delayed logical signal.

4. The line driver of claim 3 wherein the amplifier has a switching speed and the time delayed logic signal is delayed by a time substantially equal to the difference in the delay imposed by the filter and the switching speed of the amplifier.

5. The line driver of Claim 1 wherein the peak detectors is implemented as a routing running on a processor

6. The line driver of claim 5 further comprising a hold element receiving as input the logic signal or a time delayed logic signal and maintaining on an output line said logic signal or time delayed logic signal for a predetermined period of time.

7. The line driver of Claim 1 further including a peak predictor for receiving the digital data signal from the signal input and outputting an intermediate control signal.

8. The line driver of Claim 1 wherein the threshold value is associated with a proportionality between a peak value associated with the first operating voltage level and a rms value associated with the first operating voltage level.

9. The line driver of Claim 1 wherein the overhead value is determined empirically.

10. A method of operation of a line driver, comprising the steps of:

receiving a digital data signal from a signal input and outputting a first logic value when the digital data signal exceeds a threshold value and a second logic value when the digital data signal is below the threshold value, said threshold value modifiable by an overhead value;

delaying digital data signal by a programmable digital data signal delay value;

converting the digital data signal to an analog data signal;

filtering the analog data signal;

passing the filtered analog data signal to an amplifier operable at a first operating voltage level and a second operating voltage level; and

selecting between the first operating voltage level and the second operating voltage level in response to the first or second logic value.

11. The method of claim 10 further comprising programming a value for the threshold value.

12. The method of claim 8 further comprising holding the first or second logic value for a pre-determined period of time.

13. The method of claim 8 further comprising delaying the logic signal for a predetermined period of time.

14. The method of claim 13 wherein the amplifier has a switching speed and the predetermined period of time is substantially equal to the difference in the delay imposed by the filtering step and the switching speed of the amplifier.

15. The method of claim 11 wherein the threshold value is modified as a function of temperature.

16. The method of claim 10 further comprising predicting a data signal peak based upon a model of the filtering step.

17. The method of claim 10 wherein the threshold value is modified as a function of switching speed of the amplifier.

18. A line driver system, comprising:

a signal input;

a peak detector receiving a digital data signal from the signal input and outputting a logic signal having a first logic value when the digital data signal exceeds a threshold value and a second logic value when the digital data signal is below the threshold value, said threshold value modifiable by an overhead value;

a data signal delay coupled to the digital data signal input employed to output a time delayed digital data signal;

a DAC coupled to the signal input and receiving as input the digital data signal and outputting an analog data signal;

a filter receiving as input the analog data signal and outputting a filtered analog data signal;

an amplifier receiving as input the filtered analog data signal from the filter and the time delayed logic signal , the amplifier operating at a first operating voltage level when the time delayed logic signal is at the first logic value and operating at a second operating voltage level when the logic signal is at the second logic value;

a transmission line coupled to an output of the amplifier; and

a receiver coupled to an output of the transmission line.

19. The line driver system of claim 18, wherein the overhead is a programmable value.

20. The line driver system of claim 18 further comprising a logic delay receiving as input the logic signal and outputting a time delayed logic signal.

21. The line driver system of claim 20 wherein the amplifier has a switching speed and the time delayed logic signal is delayed by a time substantially equal to the difference in the delay imposed by the filter and the switching speed of the amplifier.

22. The line driver system of claim 18 further comprising a hold element coupled between said peak detector and said amplifier.

23. The line driver system of claim 22 wherein the hold element is configured to maintain the logic signal as a control input to the amplifier for a predetermined amount of time.

24. The line driver system of Claim 18 further including a peak predictor receiving as input the digital data signal from the signal input and outputting an intermediate control signal having distortion characteristics similar to the distortion characteristics of the filter.

25. The line driver system of Claim 18 wherein the threshold value is associated with a proportionality between a between a peak value associated with the first operating voltage level and an rms value associated with the first operating voltage level.

26. The line driver system of Claim 18 wherein the overhead value is determined empirically.